Remarks

With the entry of the above amendment, claims 1-19 will be pending in this case. Applicant respectfully requests that the foregoing amendments be made prior to examination of the present application. Applicant respectfully requests entry of the above amendments in order to remove multiple dependencies and correct informalities. A first office action on the merits is awaited.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,

Date: 6/30/03

Johnny A. Kumar
Attorney for Applicant
Reg. No.: 34,649

Heller Ehrman White & McAuliffe LLP
1666 K Street, N.W., Suite 300
Washington, D.C. 20006-4004
Telephone: (202) 912-2000
Facsimile: (202) 912-2020

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

[20.] 19. A ferroelectric memory device, comprising:

(2) a main cell array, including:

(A) a main bitline load controller configured to be connected between a main bitline and a positive power, and to control the flow of current in response to a second control signal, and

(B) a plurality of main sub cell blocks, each main sub block having both terminals connected to the main bitline, including:

(a) a sub bitline connected in common to a plurality of unit memory cells connected to a wordline and a plateline,

(b) a first NMOS transistor having a gate connected to a first terminal of the sub bitline and a drain connected to the main bitline,

(c) a second NMOS transistor having a gate connected to a third control signal, a drain connected to a source of the first NMOS transistor, and a source connected to ground,

(d) a third NMOS transistor having a gate connected to a fourth control signal, a drain connected to a second terminal of the sub bitline, and a source connected to ground,

(e) a fourth NMOS transistor having a gate connected to a fifth control signal, a source connected to the second terminal of the sub bitline, and a drain connected to a sixth control signal, and

(f) a fifth NMOS transistor having a gate connected to a seventh control signal, a drain connected to the main bitline, and a source connected to the second terminal of the sub bitline;

(2) a row redundancy cell array configured to share main bitlines with the main cell array;

(3) a first column redundancy cell array configured to share wordlines and platelines with the main cell array and to include redundancy main bitlines;

(4) a second column redundancy cell array configured to share redundancy wordlines and redundancy platelines with the row redundancy cell array, and to share redundancy main bitlines with the column redundancy cell array;

(5) a main bitline pull-up controller for pulling up main bitlines and redundancy main bitlines in response to first control signals, respectively;

(6) a column selection controller for connecting the main bitlines to redundancy columns and the redundancy main bitlines to main columns in response to column selection signals, respectively;

(7) a data bus unit shared by the redundancy column and the main column;

(8) a redundancy bus connected to the data bus unit shared by the redundancy column;

(9) a main bus connected to the data bus unit shared by the main column;

(10) a redundancy sense amplifier array connected to the redundancy bus; and

(11) a main sense amplifier array connected to the main bus.